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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,574	02/11/2004	Hung-Hsiang Jonathan Chao	**19-0066	2779
23377 7590 04/13/2010 WOODCOCK WASHBURN LLP CIRA CENTRE, 12TH FLOOR 2929 ARCH STREET PHILADELPHIA, PA 19104-2891				
EXAMINER SAM PHIRIN				
ART UNIT		PAPER NUMBER		
2476				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

## Application No.

10/776,574

## Applicant(s)

CHAO ET AL.

## Examiner

PHIRIN SAM

## Art Unit

2476

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 08 January 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-12, 15-26 and 28-42 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-12, 15-26, 28 and 33-42 is/are allowed.
- 6) ☒ Claim(s) 29-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 01/08/10, 02/10/10
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
3. Claims 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0131412 of Shah et al. (hereinafter "Shah") in view of US Patent 7,248,586 to Hughes, Jr. et al. (hereinafter "Hughes").

**Regarding claim 29**, Shah discloses an input module implemented in a switch, the input module comprising:

- (a) a plurality of virtual output queues for accepting cells based on cell destination information (see Fig. 1, elements 102 or 110 and 112, paragraphs [0027], [0028], the VQM 102 includes a plurality of Virtual Output Queues (VOQs). More specifically, the VQM 102 includes a unicast Virtual Output Queue (unicast VOQ) 110 and a multicast Virtual Output Queue

(multicast VOQ) 112. Incoming blocks of data to the switch system 100 can be stored (queued) in either the unicast VOQ 110 or the multicast VOQ 112 depending upon whether the incoming block is a unicast or multicast type of block. A unicast block is destined for a single destination port, while a multicast block is destined for a plurality of destination ports. By providing a separate multicast VOQ 112, the VQM 102 is able to segregate multicast blocks from unicast blocks. Such segregation allows separate processing of these different types of blocks. Typically, multicast blocks are given priority over unicast blocks);

(b) a plurality of virtual path queues for accepting cells from the plurality of virtual output queues (see Fig. 1, elements 104, 106 or 114, 116, paragraphs [0029], the VQM 104 and the VQM 106 pertain to egress paths and represent two Virtual Queue Managers that can be present on an egress side of the switch system 100. Each of the VQMs 104 and 106 includes one or more Virtual Input Queues (VIQs). In the embodiment of the switch system 100 illustrated in FIG. 1, the VQM 104 includes a VIQ 114 and the VQM 106 includes a VIQ 116);

Shah does not explicitly disclose or is silent accepting head-of-line cells from the plurality of virtual output queues, wherein each of the virtual path queues accepts a head-of line cell from a virtual output queue based on a dynamic hashing scheme. However, Hughes discloses accepting head-of-line cells, wherein each of the virtual path queues (see Fig. 3, element 350, col. 7, lines 42-53, packet reorder buffer 350 includes a head-of-line (HOL) pointer 352. HOL pointer 352 points to a packet that is stored for the longest period of time in packet reorder buffer 350. Packet reorder buffer 350 is coupled to a packet-forwarding unit 360 via a link 355. When the route lookup process of data packet 305 is completed, system 300 forwards data packet 305 to packet forwarding unit 360. After completing forwarding process for data packet 305, packet

forwarding unit 360 forwards packet 305 on an output link 365) accepts a head-of line cell based on a dynamic hashing scheme (see Figs. 1, 2a, and 3, col. 3, lines 60-67, col. 4, lines 1-11, 34-46, 51-67, col. 5, lines 1-67, and col. 6, lines 1-21). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine accepting head-of-line cells from the plurality of virtual output queues, wherein each of the virtual path queues accepts a head-of line cell from a virtual output queue based on a dynamic hashing scheme teaching by Hughes with Shah. The motivation for doing so would have been to provide to determine multiple hash values using information contained in the packets, storing the hash values in the packet reorder buffer and using the hash values to determine the second order read on column 2, lines 2-5. Therefore, it would have been obvious to combine Hughes and Shah to obtain the invention as specified in the claim 29.

**Regarding claim 30**, Shah discloses wherein the number of the plurality of virtual output queues equals a number of output ports of the switch (see Fig. 1, paragraphs [0028], [0029]).

**Regarding claim 31**, Shah discloses wherein the number of the plurality of virtual path queues equals a number of paths through a switch fabric of the switch (see Fig. 1, paragraphs [0027], [0028], and [0029]).

4. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0131412 of Shah et al. (hereinafter “Shah”) in view of US Patent 7,248,586 to Hughes, Jr. et al. (hereinafter “Hughes”) as applied to claims above, and further in view of US 2004/0246977 of Dove et al. (hereinafter “Dove”).

**Regarding claim 32**, Hughes and Shah do not explicitly disclose the number of the plurality of virtual path queues equals the number of switch planes of a switch fabric of the

switch multiplied by the number of paths through each of the switch planes. However, Dove discloses the number of the plurality of virtual path queues equals the number of switch planes of a switch fabric of the switch multiplied by the number of paths through each of the switch planes (see Fig. 1, paragraph [0046], such packet-related control and routing information includes, but is not limited to, packet type indication. RC 105, sometimes referred to as the Routing and Arbitration Processor (RAP) switch fabric, is the switching core on RAP assembly 115. The function of RAP 115 is to direct traffic from incoming ports to any outgoing port based on information maintained in RAP 115 itself or embedded within the data traffic). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the number of the plurality of virtual path queues equals the number of switch planes of a switch fabric of the switch multiplied by the number of paths through each of the switch planes teaching by Dove with Hughes and Shah. The motivation for doing so would have been to provide to support a wide variety of user interfaces, in terms of bandwidth, density, interface and application read on paragraph [0044]. Therefore, it would have been obvious to combine Dove, Hughes, and Shah to obtain the invention as specified in the claim 32.

***Allowable Subject Matter***

5. The following is a statement of reasons for the indication of allowable subject matter:

**Regarding claims 1-11**, the prior arts of record do not disclose accepting a packet associated with a flow; generating a flow group identifier from the flow; determining whether other packets associated with the flow group are present in a switch fabric; assigning the packet to a path being used by the flow group if other packets associated with the flow group are present

in the switch fabric; and assigning the packet to a path using path congestion status information if other packets associated with the flow group are not present in the switch fabric.

**Regarding claim 12**, the prior arts of record do not disclose accepting a packet associated with a flow; generating a flow group identifier from the flow; storing a first data structure in a switch fabric, the first data structure comprising a first entry the first entry comprising the flow group identifier, an outstanding packet indicator, and a path identifier; and storing a second data structure in the switch fabric, the second data structure comprising a second entry, the second entry comprising the path identifier and path status information, wherein the path status information comprises an indication of whether a path failed and an indication of whether the path is congested.

**Regarding claims 15-25**, the prior arts of record do not disclose means for accepting a packet associated with a flow; means for generating a flow group identifier from the flow; means for determining whether other packets associated with the flow group are present in a switch fabric; means for assigning the packet to a path being used by the flow group if other packets associated with the flow group are present in the switch fabric; and means for assigning the packet to a path using path congestion status information if other packets associated with the flow group are not present in the switch fabric.

**Regarding claims 26 and 28**, the prior arts of record do not assigning an incoming cell to one of the virtual output queues using cell destination information; providing a head-of-line cell of the one of the virtual output queues to one of the virtual path queues using a dynamic hashing scheme; selecting, for a switch plane link, one of a number of virtual path queues having

a cell; and sending the cell from the selected one of the number of virtual path queues over the switch plane link.

**Regarding claims 33-42**, the prior arts of record do not disclose a traffic manager module configured to: generate a flow group identifier from a flow; determine whether other packets associated with the flow group are present in the switch fabric; assign the packet to a path being used by the flow group if other packets associated with the flow group are present in the switch fabric; and assign the packet to a path using path congestion status information if other packets associated with the flow group are not present in the switch fabric.

#### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(1) US Patent 6,047,000 to Tsang et al. discloses packet scheduling system.

(2) US Patent 5,724,351 to Shao et al. discloses scaleable multicast ATM switch.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHIRIN SAM whose telephone number is (571)272-3082. The examiner can normally be reached on Increased Flexitime Policy (IFP) Program.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on (571) 272 - 3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Respectfully submitted,

Date: April 9, 2010

By: /Phirin Sam/  
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Primary Examiner  
Art Unit 2476